Remarks

The Official Action dated July 24, 2003 has been reviewed and amendments have been made as believed appropriate. The examiner's indication of allowable subject matter in claims 2 - 8 and 12 - 17 is appreciatively noted.

Claim 1 of the application stands rejected as anticipated by the Ahissar patent of record. In regard to that rejection, the examiner states that Ahissar "anticipates a weighting network having a plurality of output terminals, the weighting network having phase-based connection strengths...." The examiner cites the Ahissar abstract, Fig. 3A and col. 24 - lines 32 - 35. Applicant acknowledges that Ahissar relates to neuronal phase-locked loops. However, the Ahissar patent does not, it is urged, contain a "weighting network" like that set forth in claim 1 as currently presented. In other words, claim 1 has been amended to make it clear that the weighting network exists outside of the phase-locked loops unlike Ahissar's Fig. 3A which is Ahissar's phase-locked loop. The weighting network of claim 1 has "inputs operably coupled to outputs of the phase-locked loop and outputs operably coupled to inputs of the phase-locked loop." Nothing in the Ahissar patent suggests such an arrangement. Indeed, Ahissar makes it clear that Fig. 3A is the phase-locked loop. Referring to an excitatory phase-locked loop (ePLL) and an inhibitory phase-locked loop (iPLL), Ahissar states:

> "An ePLL is an implementation in which the PD [phase detector] excites the RCO [rate controlled oscillator] (FIG. 3A, dashed lines; FIG. 3B, AND, OR, ANDNOT and AOR), while iPLLs are those implementations in which the PD inhibits the RCO (FIG. 3A, dotted lines; FIG. 3B, NAND, NOR, NANDNOT and NAOR). Herein, AND-like and NAND-like neuronal implementations are described in detail."

With the above clarifying amendment to claim 1, it is respectfully urged that this claim now patentably differs from Ahissar.

Similarly, claim 9 stands rejected as anticipated by Ahissar. Claim 9, as well, has been amended to make it clear that the phase shift circuits are part of a weighting circuit that is exterior to the phase-locked loops being "operably connected to an input of one of the phase-locked loops." In the rejection of claim 9, the examiner points to col. 1, lines 13 - 38 of Ahissar to say that Ahissar teaches weighting elements comprising a phase shift circuit as called for by claim 9. However, col. 1, lines 13 - 38, it is clear, refers to the phase-locked loop circuit itself

and to nothing external of the phase-locked loop circuit. With the clarifying amendment to claim 9, claim 9 also clearly patentably differs from Ahissar. A further amendment to claim 9 has been made incorporating claim 1 as previously incorporated by its dependency so that claim 9 is now independent.

Claim 10 stands rejected as anticipated by Ahissar. This claim is dependent from claim 1 and incorporates the patentable features set forth in claim 1 by its dependency. Irrespective of any patentable subject matter added by claim 10, this claim, it is urged, is patentable by its dependency.

Claim 11 stands rejected as anticipated by Ahissar. The examiner refers to the abstract, FIG. 3A and columns 24, lines 32 - 35, the same parts of the Ahissar patent referred to in the rejection of claim 1. Claim 11 has also been amended for clarity. Claim 11 sets forth "each of the connectors having means for establishing a gain and a phase shift circuit." It is respectfully urged that this is unlike any connectors described by Ahissar. As rewritten, then, claim 11 is believed clearly patentable over the Ahissar patent and should be allowed at this time.

Claim 18 stands rejected as anticipated by Ahissar, the examiner pointing to col. 1, lines 9 - 12. Claim 18 is directed to a method for recognizing an incoming pattern using a neural network computer grid. It has been amended slightly for clarity such that it is now clear that it includes the step of using a phase deviation between signals representing a learned pattern and signals representing the incoming pattern. Lines 9 - 12 of col. 1 of Ahissar state:

> "The invention is directed to a novel device, called a "neuronal phase-locked loop" (NPLL), that can decode temporally-encoded information and convert it to a rate code."

Applicant respectfully urges that this statement does not refer to either a "learned pattern" or an "incoming pattern." Neither does it refer to using a phase deviation between the two patterns to arrive at an output signal indicative of the learned pattern. It is respectfully urged that claim 18 is far different from Ahissar in this respect and that the claim should be allowed at this time.

Claim 19 also stands rejected as anticipated by Ahissar. Claim 19 is dependent from claim 18 and incorporates, by its dependency, the pattentable subject matter of claim 18 discussed just above. The examiner's rejection cites to Ahissar col. 1, lines 9 - 12 and col. 6,

lines 45 - 47, but as previously stated with respect to lines 9 - 12 there is no teaching of claim 18's use of a phase deviation between patterns to create a signal indicative of a learned pattern. Likewise, col. 6, lines 45 - 47 states only:

> "The basic ePLL is a straight forward implementation of the NPLL algorithm (FIG. 2) and involves two sets of neurons: the PD and RCO sets (FIG. 3A)."

Again there is no suggestion of either a learned pattern, an incoming pattern, or the derivation of a signal that represents the learned pattern. Claim 19, like claim 18, should be found allowable at this time.

Claim 20 has been rejected over the Ahissar patent. Again the examiner cites to col. 1, lines 9 - 12. The examiner's note says "the learning is represented by how to decode and then convert." However, claim 20 refers a method of programming a neural network computer using encoding connection coefficients in accordance with the phase relationships of signals representing a pattern to be learned. Nothing of this nature is expressed in col. 1, lines 9 - 12 and it is respectfully urged that claim 20 should be allowed at this time. The amendment to claim 20 is for clarifying purposes such that it is now clear that it is signals representing a pattern whose phase relationships are used by the neural network computer.

Claims 2 - 8 and 12 - 17 were objected to as being dependent from rejected claims. Claim 2 has been rewritten in independent form and should now be allowed. Claims 3, 4 and 5 include by their dependency the subject matter of allowable claim 3 and are no longer dependent from a rejected claim. These should be allowed at this time, as well. Claim 6 has been rewritten in independent form and should therefore be allowed it is believed. Claims 7 and 8 are dependent claims that include the subject matter of claim 6, are no longer dependent from a rejected claim, and also should be allowed. Claim 12 has been rewritten in independent form and claims 13 - 16 include by their dependency the subject matter of claim 12. All of these claims are believed allowable. Claim 17 has been rewritten in independent form and should be allowed, it is urged.

Concerning the newly added claims 21 - 33, claims 21 - 23 are allowable by their dependency, incorporating therein the subject matter of claim 18. Claim 24 is dependent from claim 23 and allowable on the same basis as claim 23 in addition to any independently patentable

subject matter added by way of that claim. Claim 25 is a new independent claim that sets forth an oscillatory neural network computer having, in addition to phase-locked loop circuits, weighting circuits with "output voltages of substantially the form:

$$V(\theta) = S_{kj}*V(\theta + \psi_{kj})\ ."$$

This is unlike Ahissar and all further art of record. Allowance of claim 25 at this time is respectfully requested. Claims 26 and 27 are dependent from claim 25 and are therefore patentable with claim 25, irrespective of any independently patentable subject matter added by those claim. Claim 28 is an independent claim that sets forth the neural network being "a dynamic system that is described mathematically substantially as:

$$d\,\theta_k(t)/dt = \Omega + V(\theta_k)\sum_{j=1}^{n} S_{kj}*V(\theta_j - \pi/2)$$

for k=1,...,N, where:

θ_k is the phase of a VCO embedded in the k^{th} PLL circuit;

θ_j is the phase of the VCO embedded in the j^{th} PLL circuit;

Ω is the natural frequency of the VCO in MegaHertz (MHz);

S_{kj} are the connection strengths; and

$V(\theta)$ is a 2π periodic waveform function."

This is unlike the Ahissar neuronal phase-locked loops and any further art of record. Claim 28, it is urged, should be allowed at this point. Claims 29 and 30 incorporate by their dependency the subject matter of claim 28 and, independent of any further patentable subject matter contained therein, should be allowed at this point. Claim 31 is a further independent claim in which n^2 weighting circuits operably connect an output of each phase-locked loop to each of the n adder circuits. This is totally unlike Ahissar. No further art of record teaches such an arrangement. This claim, it is respectfully urged, is allowable at this time. Claims 31 and 33 are dependent from claim 32 and are patentable by virtue of their dependency, irrespective of any patentable content contained in those claims.

The abstract of the application has been amended slightly for clarity as will readily be apparent.

With all of the above, it is respectfully urged that this application is now in condition for allowance and further examination to that end is respectfully solicited. Should the examiner have any questions or suggestions regarding the application, he is invited to contact the undersigned attorney for applicant at the telephone number or email address set forth below.

A three-month extension of time in which to respond to the Official Action is requested in the accompanying Request for Extension. The fee for the extension of time is enclosed. However, authorization is given to charge any additional fees associated with this communication to Deposit Account No. 070135.

Respectfully submitted,

GALLAGHER & KENNEDY, P.A.

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By _____
Thomas D. MacBlain
Attorneys for Applicant
Reg. No. 24,583

Gallagher & Kennedy
2575 East Camelback Road
Phoenix, AZ 85016
(602) 530-8088
tdm@gknet.com